Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **OUT 1**
2. **IN 1-**
3. **IN 1+**
4. **V+**
5. **IN 2+**
6. **IN 2-**
7. **OUT 2**
8. **OUT 3**
9. **IN 3-**
10. **IN 3+**
11. **V-**
12. **IN 4+**
13. **IN 4-**
14. **OUT 4**

**.090”**

**.090”**

**LF**

**147H**

**MASK**

**REF**

**14 13 12**

**11**

**10**

**9**

**8**

**1**

**2**

**3**

**4**

**5 6 7**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: V-**

**Mask Ref: LF147 H**

**APPROVED BY: DK DIE SIZE .090” X .090” DATE: 11/9/21**

**MFG: NATIONAL THICKNESS .015” P/N: LF147**

**DG 10.1.2**

#### Rev B, 7/19/02